Data throttling procedures for the STS-XYTER based read-out of the CBM Silicon Tracking System

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In high interaction rate experiments using a continuous beam such as the Compressed Baryonic Matter experiment CBM at FAIR, beam intensity fluctuations are a critical issue. When such fluctuations occur, they will lead to a sudden increase in occupancy in the detector. For detector systems closest to the target such as the Silicon Tracking System STS, this may result in a local or even global overload situation, where the read-out bandwidth cannot cope with the incoming data load. In consequence, incomplete event information may be transmitted.

In conventional, triggered systems overload situations are handled by common dead time mechanisms which discard the affected fraction of events. In continuous beam experiments with freely streaming readout, however, no such trigger is available and overload would lead to uncontrolled data losses that might yield the collected data overall as none analyzable. Apart from event overlap and local pile-up, the fundamental question may be stated as: "How can one register all the data of most of the events rather than most of the data of all the events." In order to prevent complete clogging of the data chain, a throtteling mechanism is needed, that allows to inhibit acquisition of data from scrambled, not interpretable events in favour of clearing the data path for uncompromized sets of event data, once the overload condition has cleared.

In the STS the STS-XYTER read-out ASIC will be used [1]. This read-out chip is a dedicated custom design for the STS. Each readout channel is equipped with a 5 bit flash ADC. The statistically incoming hits are buffered in a per channel fifo eight levels deep and subsequently read out using a token ring scheme that is set-up to have oldest data read-out first.

Clearly, every single channel may, by pure statistical fluctuations, suffer signal pile-up or even a fifo overflow. This situation will be marked to the adjacent data elements but is not the key issue demanding throtteling. It is rather the situation of a sudden, potentially regularly appearing intensity increase that yields the average data load to be higher than the readout bandwidth. In such a situation, good data in the queue should still be read-out, but data belonging to potentially incomplete events should not cause an uncontrollable system deadtime before new data may be taken upon recovery. Further, the system should resume operation coherently.

To this end various measures have been foreseen in the design of the readout ASIC:

- Pile-up and fifo-overflow are indicated on the data elements of the particular channel.
- Channel fifo overflow conditions are counted on the chip and will realease a response report when beyond some configurable level.
- Fifos may be cleared coherently through a command.

The protocol for communication with the ASIC [2] was designed to ensure fast transfer of both the fill status reports from the ASICs and of the required responses (commands to stop -for emptying fifos- and to restart acquisition or for fast clearing of fifos).

The above provisions in the ASIC will allow to identify a problematic situation, realize throtteling as well as a coherent DAQ restart from a global control point such as the data processing board (DPB) layer through various mechanisms. No further complicated logic is needed nor foreseen in the radiation exposed front-end electronics. All further steps in the evaluation of throttling conditions can be flexibly implemented in the FGPA based DPB layer [3] based on the dedicated throttling information provided by the ASICs and on information gained directly from monitoring the ASIC hit data stream, for example indications on the ASIC fifo fill state from the difference between readout time and creation time of individual hits.

A simulation model was developed using the hardware description language SystemC [4] and some simulative prestudies have been carried out. The model currently implements a simplified structure of an STS-XYTER ASIC and allows to investigate throttling by variation of parameters like event rate, channel fifo overflow thresholds and timing of global throttling decisions. Additional simulations need to be realized to verify adequate system performance through such throttelling strategies.

References

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